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10/828,475	04/21/2004	Yoshihisa Dotta	1035-506	7094

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/828,475	DOTTA ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-9 and 17-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9 and 17-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 28 is rejected under 35 U.S.C. 102(e) as being anticipated by Hayakawa (6,450,621).

Hayakawa teaches in figures 13B and 13A and related text a semiconductor apparatus, comprising:

a semiconductor substrate 1;

a field oxide film 15 formed over a surface of the semiconductor substrate, the field oxide film having an aperture section;

a pad electrode 21 (see figure 12) over the field oxide film so as to overlap the field oxide film when perpendicularly viewing the semiconductor substrate, and

a penetration electrode 51 electrically connected to the pad electrode 32, the penetrating electrode being provided so as to pass through each of the aperture section of the field oxide film, and a hole formed in the semiconductor substrate, and

the hole in the semiconductor substrate being formed entirely in the aperture section of the field oxide film, when perpendicularly viewing the semiconductor substrate, so that an opening of the hole is smaller than the aperture section.

Claims 1-2, 4-9, 17-26 and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Mashino et al. (6,699,787).

Mashino et al. teach in figure 10 and related text a semiconductor apparatus, comprising:

a semiconductor substrate 201;

a field oxide film 204 formed over a surface of the semiconductor substrate, the field oxide film having an aperture section;

a pad electrode 211, having an aperture section formed there-through, the pad electrode being formed over the field oxide film so as to overlap the field oxide film when perpendicularly viewing the semiconductor substrate, and

a penetration electrode 217 electrically connected to the pad electrode 211, the penetrating electrode being provided so as to pass through each of (a) the aperture section of the field oxide film, (b) a hole formed in the semiconductor substrate, and (c) the aperture section of the pad electrode,

the hole in the semiconductor substrate being formed in the aperture section of the field oxide film, when perpendicularly viewing the semiconductor substrate, so that an opening of the hole is smaller than the aperture section of the field oxide film,

wherein the penetration electrode is formed in a field area of the surface of the semiconductor substrate,

wherein the aperture section of the field oxide film is formed in the aperture section of the pad electrode, when perpendicularly viewing the semiconductor substrate,

wherein the penetration electrode includes a hole-filling section formed in the hole,

wherein the hole-filling section is made of an electrically conductive material,

wherein a pad electrode formed so that there is no overlap with the hole when perpendicularly viewing the semiconductor substrate.

Regarding claims 5-6, Mashino et al. teach in figure 10 and related text an insulating film 209 is formed on an internal surface of the hole, between the internal surface of the hole and a sidewall of the penetration electrode,

Regarding claims 6, 8 and 22-23, Mashino et al. teach in figure 10 and related text a penetration electrode includes an electrically conductive film 16 on the insulating film that is formed on the internal surface of the hole,

wherein the hole-filling section is made of an insulating material and of an electrically conductive material,

wherein the insulating film is in direct contact with the field oxide film,

wherein the pad electrode is formed directly on and contacting the field oxide film.

Regarding claim 21, Mashino et al. teach in figure 10 and related text the aperture section in the pad electrode is larger than the aperture section in the field oxide film, when perpendicularly viewing the semiconductor substrate, because the aperture section in the pad electrode can be arbitrarily chosen to be larger than the aperture section in the field oxide film.

Regarding claims 24-26, Mashino et al. teach in figure 10 and related text a penetration electrode extends through the aperture section of the pad electrode is located at elevations both above and below the pad electrode.

Claims 1-2, 4-9, 17-26 and 28 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art (AAPA).

AAPA teaches in figures 16-17 and related text a semiconductor apparatus, comprising:

a semiconductor substrate 101;

a field oxide film 102 formed over a surface of the semiconductor substrate, the field oxide film having an aperture section;

a pad electrode 104, having an aperture section formed there-through, the pad electrode being formed over the field oxide film so as to overlap the field oxide film when perpendicularly viewing the semiconductor substrate, and

a penetration electrode 115 electrically connected to the pad electrode 104, the penetrating electrode being provided so as to pass through each of (a) the aperture section of the field oxide film, (b) a hole formed in the semiconductor substrate, and (c) the aperture section of the pad electrode,

the hole in the semiconductor substrate being formed in the aperture section of the field oxide film, when perpendicularly viewing the semiconductor substrate, so that an opening of the hole is smaller than the aperture section of the field oxide film,

wherein the penetration electrode is formed in a field area of the surface of the semiconductor substrate,

wherein the aperture section of the field oxide film is formed in the aperture section of the pad electrode, when perpendicularly viewing the semiconductor substrate,

wherein the penetration electrode includes a hole-filling section formed in the hole,

wherein the hole-filling section is made of an electrically conductive material,

wherein a pad electrode formed so that there is no overlap with the hole when perpendicularly viewing the semiconductor substrate.

Regarding claims 5-6, AAPA teaches in figures 16-17 and related text an insulating film 109 is formed on an internal surface of the hole, between the internal surface of the hole and a sidewall of the penetration electrode,

Regarding claims 6, 8 and 22-23, AAPA teaches in figures 16-17 and related text a penetration electrode includes an electrically conductive film on the insulating film that is formed on the internal surface of the hole,

wherein the hole-filling section is made of an insulating material and of an electrically conductive material,

wherein the insulating film is in direct contact with the field oxide film,

wherein the pad electrode is formed directly on and contacting the field oxide film.

Regarding claim 21, AAPA teaches in figures 16-17 and related text the aperture section in the pad electrode is larger than the aperture section in the field oxide film, when perpendicularly viewing the semiconductor substrate, because the aperture section in the pad electrode can be arbitrarily chosen to be larger than the aperture section in the field oxide film.

Regarding claims 24-26, AAPA teaches in figures 16-17 and related text a penetration electrode extends through the aperture section of the pad electrode is located at elevations both above and below the pad electrode.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mashino et al. or AAPA.

Regarding claim 27, Mashino et al. and AAPA teach substantially the entire claimed structure, as applied to claim 1 above, except explicitly stating that the aperture section of the pad electrode is a hole formed through the pad electrode, such that the aperture section is surrounded by the pad electrode when perpendicularly viewing the semiconductor substrate.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the aperture section of the pad electrode as a hole formed through the pad electrode, such that the aperture section is surrounded by the pad electrode when perpendicularly viewing the semiconductor substrate., in Mashino et al. or AAPA's device in order to simplify the processing steps of making the device by forming the aperture section as a hole through the pad electrode.

Claims 1-2, 4-9, 17-28 are rejected, in the alternative, under 35 U.S.C. 103(a) as being unpatentable over Mashino et al. in view of Uehara (5,262,671).

Mashino et al. teach in figure 10 and related text a semiconductor apparatus, comprising:

a semiconductor substrate 201;

a pad electrode 211, having an aperture section formed there-through, and

a penetration electrode 217 electrically connected to the pad electrode 211, the penetrating electrode being provided so as to pass through each of (b) a hole formed in the semiconductor substrate, and (c) the aperture section of the pad electrode,

Mashino et al. do not teach a FOX region ("field oxide film"), such that:

the field oxide film having an aperture section;

a pad electrode being formed over the field oxide film so as to overlap the field oxide film when perpendicularly viewing the semiconductor substrate, and

a penetration electrode pass through the aperture section of the field oxide film,

a hole formed in the semiconductor substrate, wherein

the hole in the semiconductor substrate being formed in the aperture section of the field oxide film, when perpendicularly viewing the semiconductor substrate, so that an opening of the hole is smaller than the aperture section of the field oxide film.

Uehara teaches in figures 1 and 2 and related text a FOX region ("field oxide film") 2, wherein

the field oxide film 2 formed over a surface of the semiconductor substrate 1, the field oxide film having an aperture section,

a pad electrode 6, having an aperture section formed there-through, the pad electrode being formed over the field oxide film so as to overlap the field oxide film when perpendicularly viewing the semiconductor substrate,

wherein the aperture section of the field oxide film is formed in the aperture section of the pad electrode, when perpendicularly viewing the semiconductor substrate.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a FOX region ("field oxide film") in Mashino et al.'s device in order to isolate the device from surrounding devices, by conventional method, of which official notice is taken.

Note that forming a FOX region, as taught by Uehara, in Mashino et al.'s device, would result in a device a semiconductor apparatus, comprising:

a semiconductor substrate;

a field oxide film formed over a surface of the semiconductor substrate, the field oxide film having an aperture section;

a pad electrode, having an aperture section formed there-through, the pad electrode being formed over the field oxide film so as to overlap the field oxide film when perpendicularly viewing the semiconductor substrate, and

a penetration electrode electrically connected to the pad electrode, the penetrating electrode being provided so as to pass through each of (a) the aperture section of the field oxide film, (b) a hole formed in the semiconductor substrate, and (c) the aperture section of the pad electrode,

the hole in the semiconductor substrate being formed in the aperture section of the field oxide film, when perpendicularly viewing the semiconductor substrate, so that an opening of the hole is smaller than the aperture section of the field oxide film,

wherein the penetration electrode is formed in a field area of the surface of the semiconductor substrate,

wherein the aperture section of the field oxide film is formed in the aperture section of the pad electrode, when perpendicularly viewing the semiconductor substrate,

wherein the penetration electrode includes a hole-filling section formed in the hole,

wherein the hole-filling section is made of an electrically conductive material,

wherein a pad electrode formed so that there is no overlap with the hole when perpendicularly viewing the semiconductor substrate,

an insulating film 109 is formed on an internal surface of the hole, between the internal surface of the hole and a sidewall of the penetration electrode,

a penetration electrode includes an electrically conductive film on the insulating film that is formed on the internal surface of the hole,

wherein the hole-filling section is made of an insulating material and of an electrically conductive material,

wherein the insulating film is in direct contact with the field oxide film,

wherein the pad electrode is formed directly on and contacting the field oxide film, wherein

the aperture section in the pad electrode is larger than the aperture section in the field oxide film, when perpendicularly viewing the semiconductor substrate, because the aperture section in the pad electrode can be arbitrarily chosen to be larger than the aperture section in the field oxide film, wherein

a penetration electrode extends through the aperture section of the pad electrode is located at elevations both above and below the pad electrode.

Response to Arguments

Applicant's argues that Mashino et al. do not teach a FOX region.

Applicant does not claim a FOX region. Applicant discloses and claims a field oxide film (i.e. an oxide layer). Said film or layer is depicted in the drawings as an insulating layer, and not as a FOX region.

Furthermore, using an oxide layer formed by LOCOS method is a process limitations which would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not

the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in □product by process claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

The rest of applicant's arguments were adequately addressed in previous office actions, and are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-4670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
12/10/07

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